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Claims

[c1] 1. A pixel structure, comprising:

a gate line, located on a substrate;

a common line, located on said substrate for a bottom electrode of a pixel storage capacitor;

a gate insulating layer, located on said substrate, said gate insulating layer covering said gate line and said common line;

a data line, located on said gate insulating layer;

a switching device, located on said substrate, said switching device electrically connecting said gate line and said data line;

a conducting layer, located on said gate insulating layer, said conducting layer including a coupling portion and a connecting portion, said coupling portion being above said common line for a top electrode of said pixel storage capacitor, said connecting portion connecting said coupling portion and said switching device;

a passivation layer, covering said data line, said switching device, and said conducting layer;

a contact window, disposed in said passivation layer and above said connecting portion; and

a pixel electrode, located on said passivation layer, said

pixel electrode electrically connecting said switching device and said coupling portion of said conducting layer through said contact window.

[c2] 2. The pixel structure of claim 1, wherein said connecting portion of said conducting layer is a multi-channel structure, said connecting portion comprising:
a first portion coupled to said coupling portion;
a second portion connected to said switching device; and
a third portion between said first portion and said second portion, said third portion including a plurality of channels.

[c3] 3. The pixel structure of claim 2, wherein said contact window is disposed in said passivation layer and above one of said plurality of channels of said third portion.

[c4] 4. The pixel structure of claim 1, further comprising a blocking layer below said connecting portion.

[c5] 5.The pixel structure of claim 1, further comprising a planarization layer between said passivation and said pixel electrode.

[c6] 6.The pixel structure of claim 1, wherein said switching device is a thin film transistor, said thin film transistor comprising:
a gate electrode electrically connected to said gate line;

a channel layer on the gate insulating layer above said gate electrode;
a source electrode and a drain electrode on said channel layer, said source electrode being electrically connected to said data line, said drain electrode being electrically connected to said connecting portion of said conducting layer.

[c7] 7.The pixel structure of claim 1, wherein said gate line is parallel to said common line.

[c8] 8.A method of fabricating a pixel structure, comprising sequentially forming a gate electrode a gate line and a common line on a substrate, wherein the gate line is electrically connected to said gate electrode;
forming a gate insulating layer on said substrate to cover said gate electrode, said gate line and said common line;
forming a channel layer above said gate insulating layer and said gate electrode;
forming a data line and a conducting layer on said gate insulating layer and forming a source electrode and a drain electrode on said channel layer, said data line being electrically connected to said source electrode, said conducting layer including a coupling portion and a connecting portion, said coupling portion being formed above said common line, said connecting portion connecting said coupling portion and said drain electrode;

forming a passivation layer above said substrate covering said data line, said conducting layer and said thin film transistor;
forming a contact window in said passivation layer exposing said connecting portion; and
forming a pixel electrode on said passivation layer, said pixel electrode being electrically connected to said conducting layer through said contact window.

[c9] 9. The method of claim 8, wherein said connecting portion of said conducting layer includes a plurality of channels.

[c10] 10. The method of claim 9, wherein said contact window exposes one of plurality of channels of said connecting portion.

[c11] 11. The method of claim 8, further comprising forming a blocking layer below said contact window and said connecting portion.

[c12] 12. The method of claim 11, wherein said blocking layer is formed in a common area during forming said gate electrode, said gate line, and said common line..

[c13] 13. The method of claim 8, before the step of forming said pixel electrode, further comprising forming a planarization layer on said passivation..

[c14] 14. The method of claim 8, wherein common line is parallel to said gate line.